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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/842,435	04/25/2001	Brian William Hughes	10004546-1	7471

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/842,435	HUGHES ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-29* is/are pending in the application.

4a) Of the above claim(s) *11-17 and 21-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 21-29 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claim 21 recites, "successively scanning each of a plurality of subsets of said memory segment, wherein each said subset comprises at least two linear arrays of elements", which is properly classified in 714/746. Claims 21-29 are directed to a method for scan testing subsets of a memory segment different from the system of Group I which is directed to a system for tracking and generating counts of identified faults in a memory (properly classified in 714/723) and the method of Group II which is a method for preserving an operation of a memory segment by comparing a determined number of identified faults of evaluated elements to a fault threshold value and re-mapping said memory segment in response to a declared failure condition (properly classified in 714/711). Note: claim 21 is directed to scan testing of subsets of said memory segment comprising two linear arrays of elements whereas claim 18 is directed to evaluating after scan testing.

Inventions claims 21-29 and Group I are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case, the process of claims 21-29 can be practiced by a

scan testing device. In this case, the system of Group I can be used in a method for logging faults.

Inventions Group II and Claims 21-29 are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group II has separate utility such as for use in a comparison test for comparing a determined number of identified faults of evaluated elements to a fault threshold value. In the instant case, invention Claims 21-29 has separate utility such as for scan testing subsets of a memory segment. See MPEP § 806.05(d).

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 21-29 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 11-17, drawn to A system for maintaining an operation of a memory segment comprising a means for evaluating elements of a plurality of subsets of said memory segment in row-fast order wherein each said subset is at least two linear arrays of said elements and a

means for generating a count of identified faulty ones of evaluated elements found for each subset of said memory segment wherein said generating means is operative to act successively through said plurality of subsets, classified in class 714, subclass 723.

II. Claims 18-20, drawn to A method for preserving an operation of a memory segment comprising the steps of comparing a determined number of identified faulty ones of evaluated elements to a fault threshold value and physically re-mapping said memory segment in response to said declared failure condition, classified in class 714, subclass 711.

The inventions are distinct, each from the other because of the following reasons: Inventions Group II and Group I are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the apparatus, Group I, can be used strictly for self-testing comprising a means for evaluating elements of a plurality of subsets of said memory segment in row-fast order wherein each said subset is at least two linear arrays of said elements and a means for generating a count of identified faulty ones of evaluated elements found for each subset of said memory segment wherein said generating means is operative to act successively through said plurality of subsets and the process, Group II, can be used in a self repair system comprising a means for

evaluating elements of a plurality of subsets of said memory segment in row-fast order wherein each said subset is at least two linear arrays of said elements and a means for generating a count of identified faulty ones of evaluated elements found for each subset of said memory segment wherein said generating means is operative to act successively through said plurality of subsets.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Michael Papalas on 28 September 2004 a provisional election was made with traverse to prosecute the invention of Group II, claims 18-29. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-17 and 21-29 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.
This application contains claims 11-17 and 21-29 drawn to nonelected inventions. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

3. In view of corrections to the drawings in the amendment filed 30 August 2004, all objections to the drawings are withdrawn.

Specification

4. In view of corrections to the specification in the amendment filed 30 August 2004, all objections to the specification are withdrawn.

Claim Rejections - 35 USC § 112

5. In view of corrections to claims 18-20 in the amendment filed 30 August 2004, all 35 USC § 112 rejections to claims 18-20 are withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton) in view of Harns; Timothy (US 4460997 A).

35 U.S.C. 103(a) rejection of claim 18.

Eaton teaches evaluating elements of a memory segment (col. 4, lines 41-47 in Eaton teach that Figure 3 of Eaton is comprises of IC chips 3-1; Note: an IC chips 3-1 in Figure 3 is a memory segment); identifying faulty ones of said evaluated elements (col. 7, lines 5-15 in Eaton teach that ECC Engine 3-3 of Figure 3 in Eaton is used to identify hard and soft errors at a memory location or cell; Note: a memory location or cell is a memory element and a means for determining a hard error is means for determining a faulty memory cell since hard errors are errors due to defective memory elements); determining a number of said identified faulty ones of said evaluated elements in each of a plurality of subsets of said memory segment (col. 5, lines 61-68 in Eaton teach that that each IC chip 3-1 in Figure 3 stores data records in subsets of the IC chip 3-1; col. 7, lines 14-17 in Eaton teaches that the ECC engine 3-3 is used to determine the number of defects in a record; Note: a record is substantially a subset of a IC chip memory segment 3-1); comparing said determined number to a fault threshold value (col. 7, lines 17-21 in Eaton teaches that if the number of defects exceeds a criterion for acceptable ECC engine 3-3 margin; Note: a criterion for acceptable ECC engine 3-3 margin is a threshold); declaring a failure condition for said memory segment if said determined number is greater than equal to said fault threshold value for any column of said memory segment (col. 7, lines 17-21 in Eaton teaches that if the number of defects exceeds, i.e., is greater than or equal to, a threshold for acceptable ECC engine 3-3 margin, then that group of defective memory cells is taken out of use, i.e., a failure for said memory segment is declared); and physically re-mapping said memory segment in response to said declared failure condition (col. 7, lines 21-24 in Eaton teaches that the

group of declared defective memory cells are taken out of use and replaced or remapped to replacement memory cells 3-5c in Figure 3).

However Eaton does not explicitly teach the specific use of evaluating elements of said memory segment in row-fast order.

Harns, in an analogous art, teaches evaluating elements of said memory segment in row-fast order (col. 32, lines 12-15, Harns). Note: Eaton teaches testing and evaluating memory elements of a memory system but does not teach the details of how data is read out of memory during testing. Harns, on the other hand, teaches a commonly know means for reading data out of memory. One of ordinary skill in the art at the time the invention was made would have been highly motivated to combine Eaton with Harns in order to provide a means for reading data out of memory in the Eaton patent. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Eaton with the teachings of Harns by including use of evaluating elements of said memory segment in row-fast order. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of evaluating elements of said memory segment in row-fast order would have provided the means for reading data out of memory (col. 32, lines 12-15, Harns).

35 U.S.C. 103(a) rejection of claim 19.

The Examiner asserts that col. 5, lines 61-68 of Eaton teaches Reed-Solomon ECC check bits are used to check integrity of data after stored evaluation data is read out of

an nxm memory cell array segment. One of ordinary skill in the art at the time the invention was made would have known that error checking for data d with check-bits c occurs by re-encoding data d to produce re-encoded expected check-bits c' whereby c' is compared to c to determine if an error has occurred (Note: comparing c to c' is equivalent to comparing stored d+c to expected data d+c', hence comparing c to c' is a step for comparing read stored evaluation data to expected data).

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eaton; Steven G. et al. (US 4939694 A, hereafter referred to as Eaton) and Harns; Timothy (US 4460997 A).

35 U.S.C. 103(a) rejection of claim 20.

Eaton and Harns substantially teaches the claimed invention described in claims 18 and 19 (as rejected above).

However Eaton and Harns do not explicitly teach the specific use of a failure counter. The Examiner asserts that col. 7, lines 14-17 in Eaton teaches that the ECC engine 3-3 is used to determine the number of defects in a subset. One of ordinary skill in the art at the time the invention was made would have known that a counter is a means for determining a number of defects in a subset. Note: the count only has to be retained for analysis of a record and afterwards must be reset to evaluate a new record in Eaton. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Eaton and Harns by including use of a

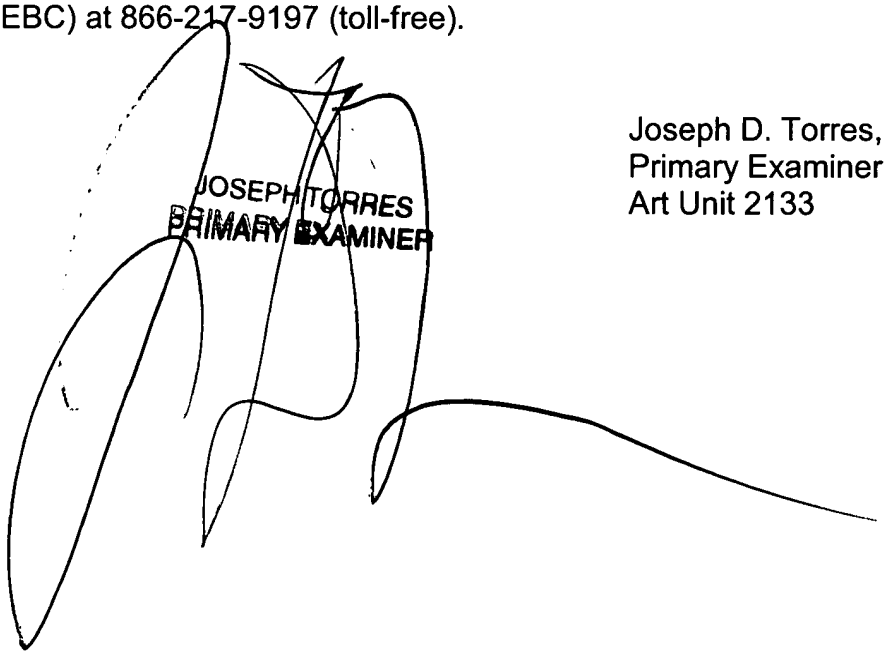
failure counter. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a failure counter would have provided the opportunity to implement the means for determining a number of defects in a subset taught in the Eaton patent (col. 7, lines 14-17 in Eaton teaches that the ECC engine 3-3 is used to determine the number of defects in a subset).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Art Unit 2133